Session 25 Overview

RF/IF Circuits

Chair: Tom Schiltz, Linear Technology, Colorado Springs, CO

Associate Chair: Satoshi Tanaka, Hitachi, Tokyo, Japan

Increasing popularity of wireless devices, including cellular phones, wireless LAN and other data services, is placing higher performance demands on the radio portion of these devices. Lower noise and higher linearity are the primary performance improvements needed in the RF and IF circuits to expand the dynamic range, and allow operation in these congested radio channels.

The eight presentations in this session highlight specific RF and IF circuit improvements that enhance dynamic range, thus permitting further growth of wireless. These improvements are realized primarily through novel circuit designs, enabled by silicon processing improvements.

A critical block in radio transmitters, the upmixer, is known to produce a broad spectrum of undesired output frequencies, in addition to the desired output. Expensive filtering is normally employed to attenuate the undesired spurious outputs prior to transmission. Paper 25.1 presents a unique upmixer topology that suppresses these undesired harmonics and sidebands to less than -40dBc, thus allowing relaxed filtering in a transmitter.

Papers 25.2 and 25.3 detail circuit techniques that improve image rejection in receivers. Both techniques incorporate automatic calibration schemes to balance the I- and Q-path gains, and optimize phase quadrature.

Solutions to improve the 2nd-order rejection in direct conversion receivers are presented in Papers 25.4 and 25.7. Measurements show IIP2 improvements of 18 to 20dB in both cases.

A unique bias-control scheme for an active channel-select filter is presented in Paper 25.6, which adapts the bias current depending on the level of a blocking signal.

The session concludes with two papers that present improved direct I/Q demodulator performance. Paper 25.5 utilizes a local oscillator at one-half the normal frequency to reduce LO leakage at the RF input to -91dBm. Paper 25.8, on the other hand, uses an LO at twice the normal frequency to reduce 1/f noise contributions, resulting in a 9dB NF improvement.

25.1 A Multipath Technique for Canceling Harmonics and Sidebands in a Wideband Power Upconverter **8:30 AM**
R. Shrestha, University of Twente, Enschede, The Netherlands

Switching mixers are power-efficient but produce unwanted harmonics and sidebands. A multipath technique to clean up the spectrum using digital circuits and mixers, but no filters, is applied to a 0.13µm CMOS power upconverter. The circuit delivers 8mW from dc to 2.4GHz with 11% drain efficiency, with spurs <-40dBc over more than 4 octaves in frequency, and consumes 228mW from a 1.2V supply.

25.2 A Complex Image-Rejection Circuit with Sign Detection Only **9:00 AM**
S. Lerstaveesin, University of California, San Diego, La Jolla, CA

The orthogonal property of I/Q channels is applied to adaptively correct path gain and phase errors using four sign detectors. A complex baseband S/H chip achieves an image rejection of 65dB while sampling at 40MS/s. The chip occupies 0.8×0.45mm^2 in a 0.18µm CMOS process and consumes 23mW at 1.8V.

25.3 On-Chip Image Rejection in a Low-IF CMOS Receiver **9:30 AM**
M. Hajirostam, University of Toronto, Toronto, Canada

An adaptive image-reject mixer is realized in a 0.18µm CMOS technology. The circuit achieves high image-rejection ratios without off-chip filters in applications such as TV tuners. Test results show a 54dB image-rejection ratio in a low-IF receiver. The circuit consumes 75mW from a 1.8V supply and occupies 2.25mm^2 including pads.

25.4 Active 2nd-Order Intermodulation Calibration for Direct-Conversion Receivers **10:15 AM**
M. Chen, University of California, Los Angeles, CA

A temperature-compensated active IM2 calibration circuit for direct-conversion receivers is fabricated with a mixer in 0.25µm CMOS. A squaring circuit senses the RF signal and generates a calibration current to cancel mixer IM2 distortion. The loading effect and noise contribution are minimized by gain boosting. IIP2 is boosted >20dB to >80dBm in the IMT band. The calibration circuit draws 1.5mA.

25.5 A 2.2GHz Sub-Harmonic Mixer for Direct-Conversion Receivers in 0.13µm CMOS **10:45 AM**
H. Jen, University of California, Berkeley, CA

A 0.13µm CMOS sub-harmonic mixer uses a passive switching network to achieve a dc offset of 0.7mV and a 2×LO leakage of -91dBm at the RF port. The LO leakage is -95dBm, and the flicker-noise corner is 100kHz. The mixer requires an LO input power of -18dBm and consumes 13mW from a 1.2V supply.

25.6 A Blocker-Vigilant Channel-Select Filter with Adaptive IIP3 and Power Dissipation **11:15 AM**
A. Yoshizawa, Columbia University, New York, NY

A dynamic biasing scheme that reduces the average dc power of channel-select filters is presented. An adaptive IIP3, 5th-order Butterworth low-pass filter is implemented in a 0.18µm CMOS process with a 1.8V supply voltage. The filter quiescent current is 1.2mA, with a -5dBV out-of-channel IIP3. With a blocker level of -13dBV, the supply current increases to 2.7mA and the IIP3 increases to +20dBV.

25.7 An IP2 Improvement Technique for Zero-IF Down-Converters **11:45 AM**
H. Darabi, Broadcom, Irvine, CA

An IP2 calibration circuit to improve the 2nd-order nonlinearity of mixers in zero or low-IF receivers is presented. The circuit allows the mixers to be optimized independently, and has negligible impact on receiver noise figure, area, and power consumption. A prototype transceiver including the calibration circuitry in 0.13µm CMOS is fabricated. An average IIP2 improvement of 18dB is measured.

25.8 Low Flicker-Noise Quadrature Mixer Topology **12:00 PM**
R. Pullela, Skyworks Solutions, Irvine, CA

A mixer topology that improves NF at low offset frequencies by reducing 1/f noise contributions is fabricated in 0.13µm CMOS. The NF at 10kHz is 9dB, which is 9dB less than a conventional mixer. The mixer also has 2dB higher gain, improved quadrature matching, higher IP2, straightforward implemention, and is robust over PVT.